New Pipeline DAQ
and
12GeV Trigger Systems

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Hall C Summer Workshop
Jefferson Lab
15-August-2013

OUTLINE

- **Overview -**
  - **DAQ and Trigger design requirements**
  - **Before Pipeline – The Classic method of DAQ**
  - **Extension of VME with high speed Gigabit Serial (VXS or VITA-41)**
  - **Hardware Acronym Definitions**
  - **Trigger System Hardware, Methods and Examples**

- **Hardware Status**
  - **Production Board updates**
  - **System Test Activities, Results and New Applications**
    - **New DAQ hardware successfully used for Heavy Photon Search beam test June 2012**
    - **Hall Detector groups using new boards for commissioning**

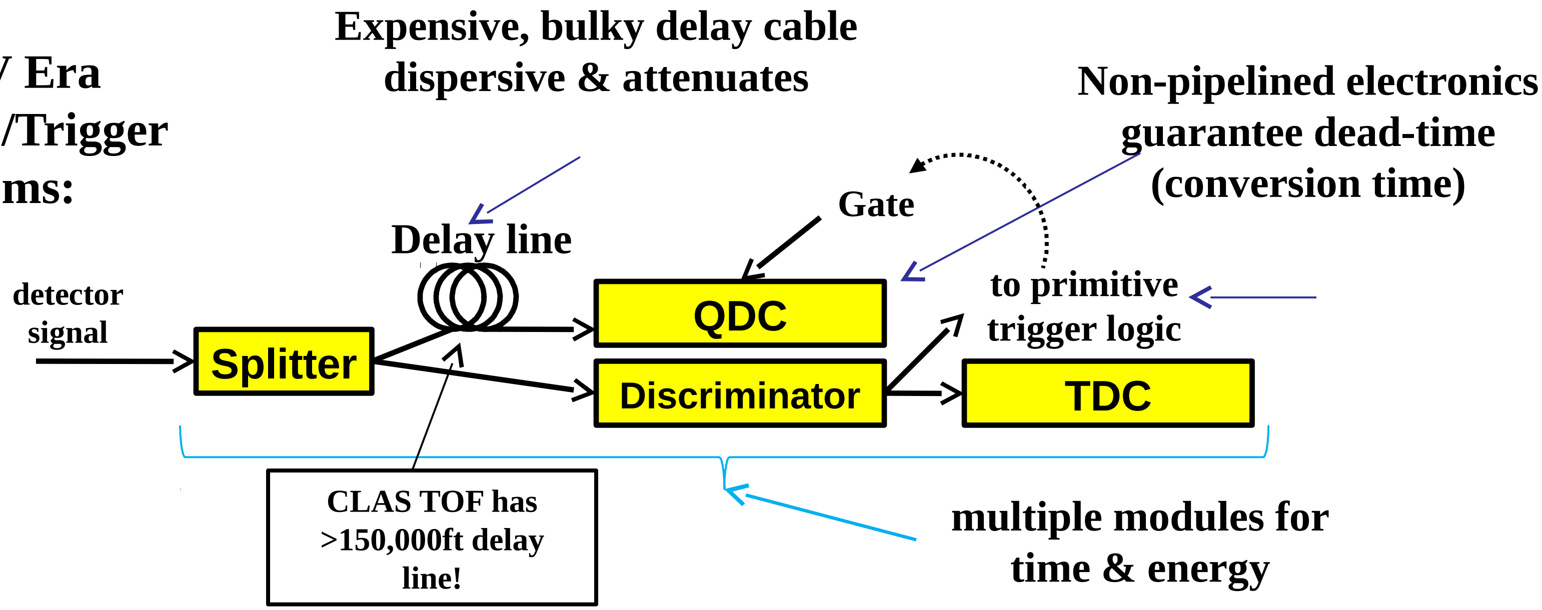
- **Summary**

Main Trigger Design Requirements

- **200kHz average (Hall D) Level 1 Trigger Rate, Pipelined with up to 8μs front end digitizer memory**
  - **High Luminosity -> $10^8 \gamma/s$ creates high average trigger rate**
  - **Initial commissioning at low beam current (~200nA). Luminosity - $10^7 \gamma/s$**
- **L1 trigger supports pipelined subsystem hit patterns and energy summing with low threshold suppression**
- **Scalable trigger distribution scheme (Up to 128 crates)**
  - **Hall D: 25 L1 Trigger crates, 52 total readout crates**
  - **Hall B: 38 L1 Trigger crates, 56 total readout crates**
  - **Hall A & C will have < 2 L1 Trigger crates**
- **Low cost front-end & trigger electronics solution**
- **Strong FIRMWARE Features –**
  - **Hall B will use different programmable features than Hall D**
  - **Strong Partnership between Detector Groups and Firmware experts**
  - **Firmware "QA" control In Electronics/DAQ groups**
  - **Firmware can be remotely loaded to FPGAs from VME**
- **<u>ALL</u> Halls will benefit from new hardware design solutions**

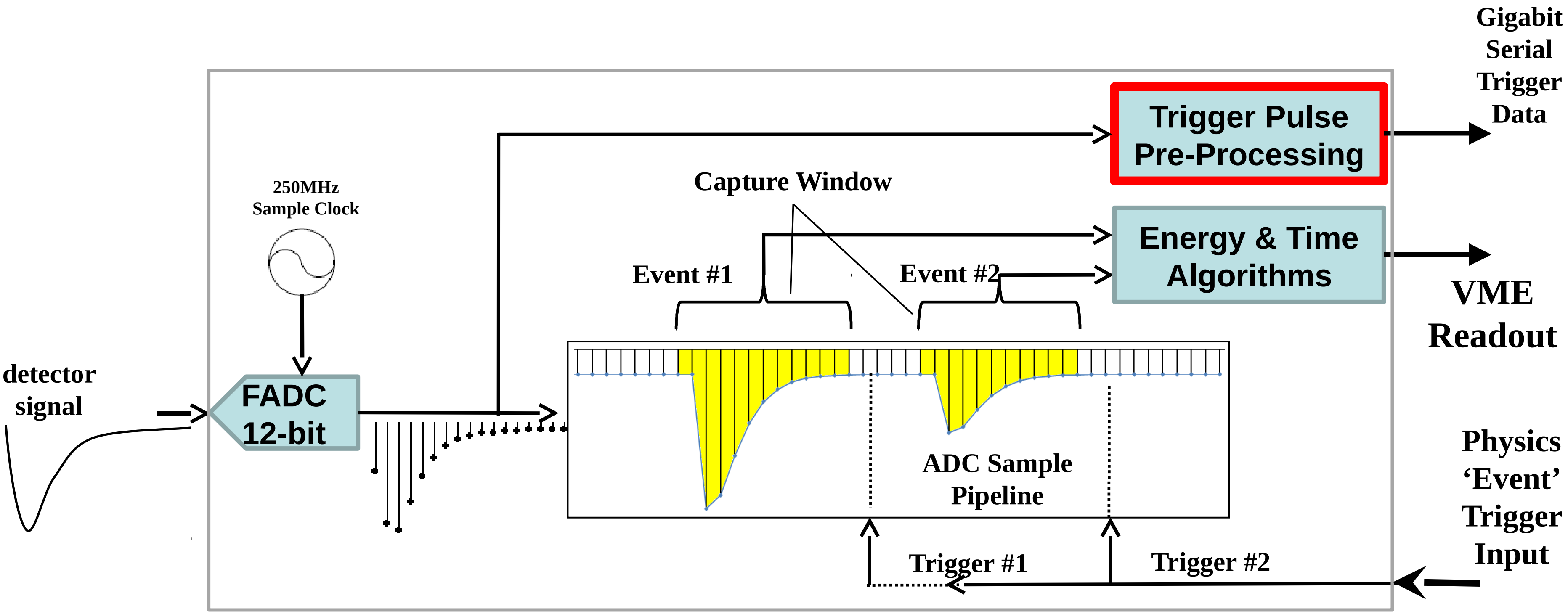
The “Classical” method to capture detector signals

6GeV Era DAQ/Trigger Systems:



“Classic” DAQ Electronic examples:
FastBus 1881 QDC
FastBus 1887 TDC
Many NIM modules for Trigger Logic

Modern Method of Signal Capture



- 250MHz Flash ADC stores digitized signal in 8µs circular memory
- "Event" trigger extracts a window of the ADC data for <u>pulse sum</u> and <u>time algorithms</u>
- Trigger data contains detailed information useful for cluster finding, energy sum, etc.
- Hardware algorithms provide a huge data reduction by reporting only time & energy estimates for readout instead of raw samples

Acronym Definitions

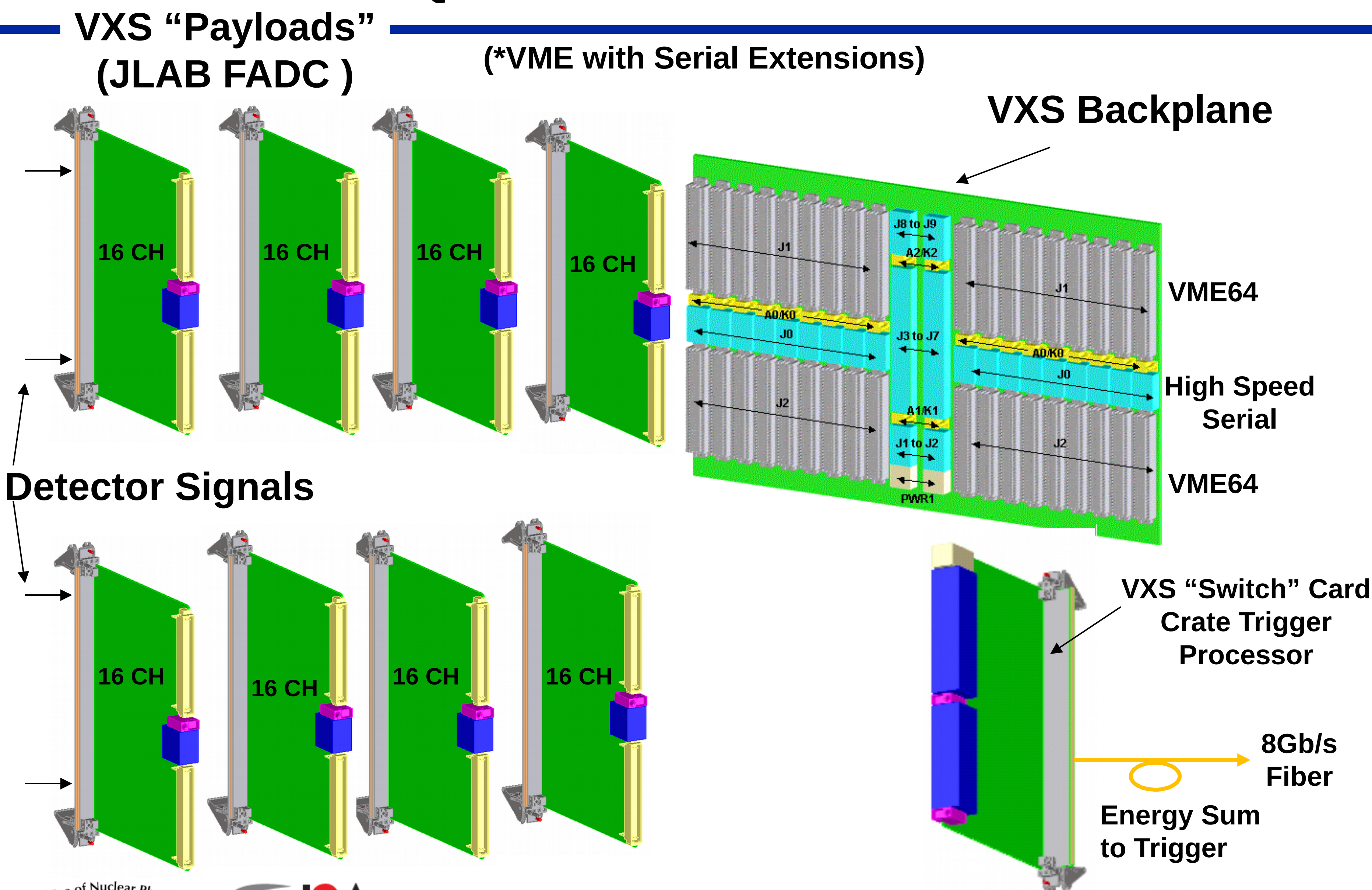
- **VXS => VME with Serial Extensions (VITA 41.0)**
- **VITA => VME International Trade Association**

- **FADC250 => Flash Analog to Digital Converter 250MHz**
- **CTP => Crate Trigger Processor**
- **TI => Trigger Interface**
- **SD=> Signal Distribution**

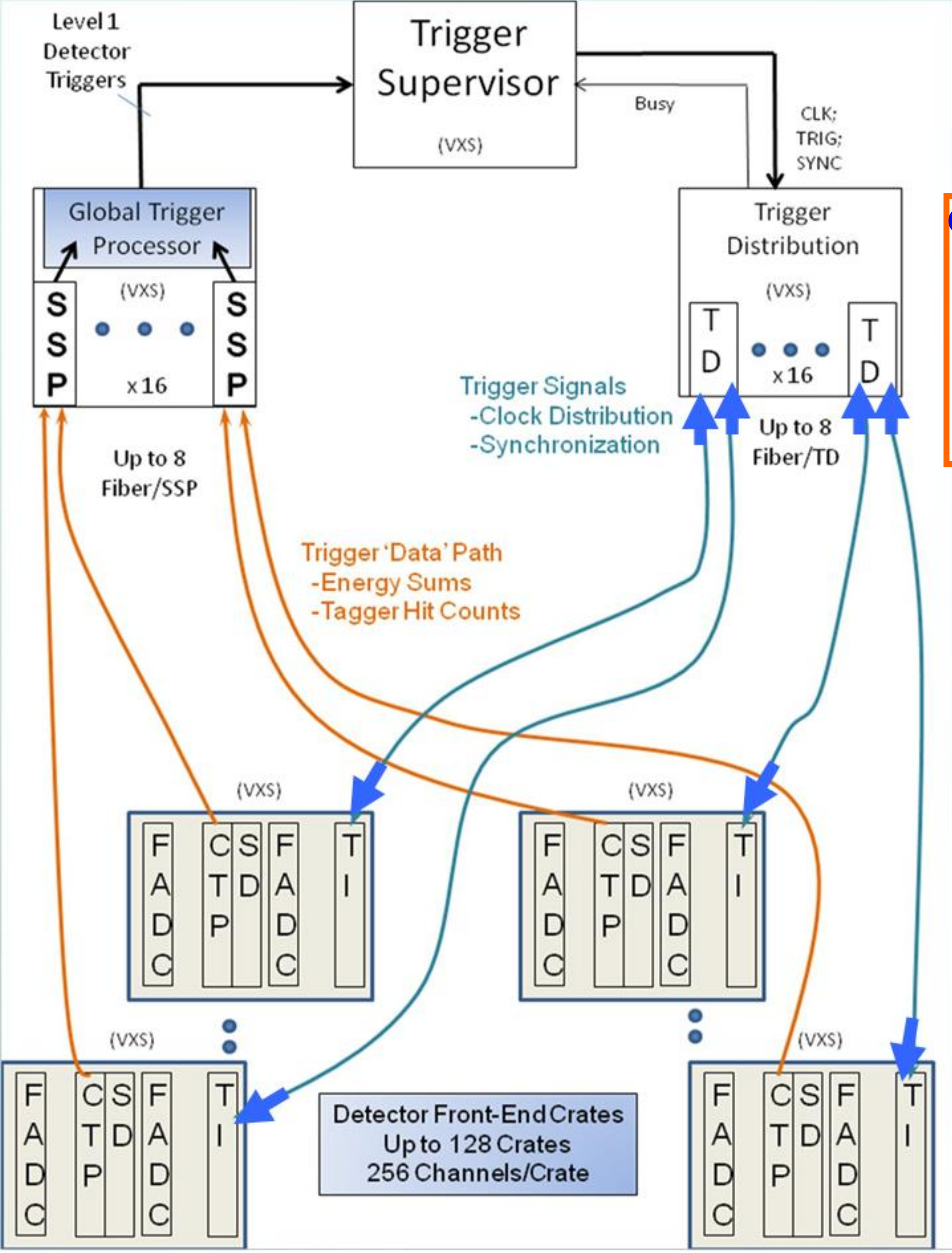
- **SSP=> Sub_System Processor**
- **GTP=> Global Trigger Processor**
- **TS=> Trigger Supervisor**
- **TD=> Trigger Distribution**

Quick VITA 41 *VXS Review_

(*VME with Serial Extensions)

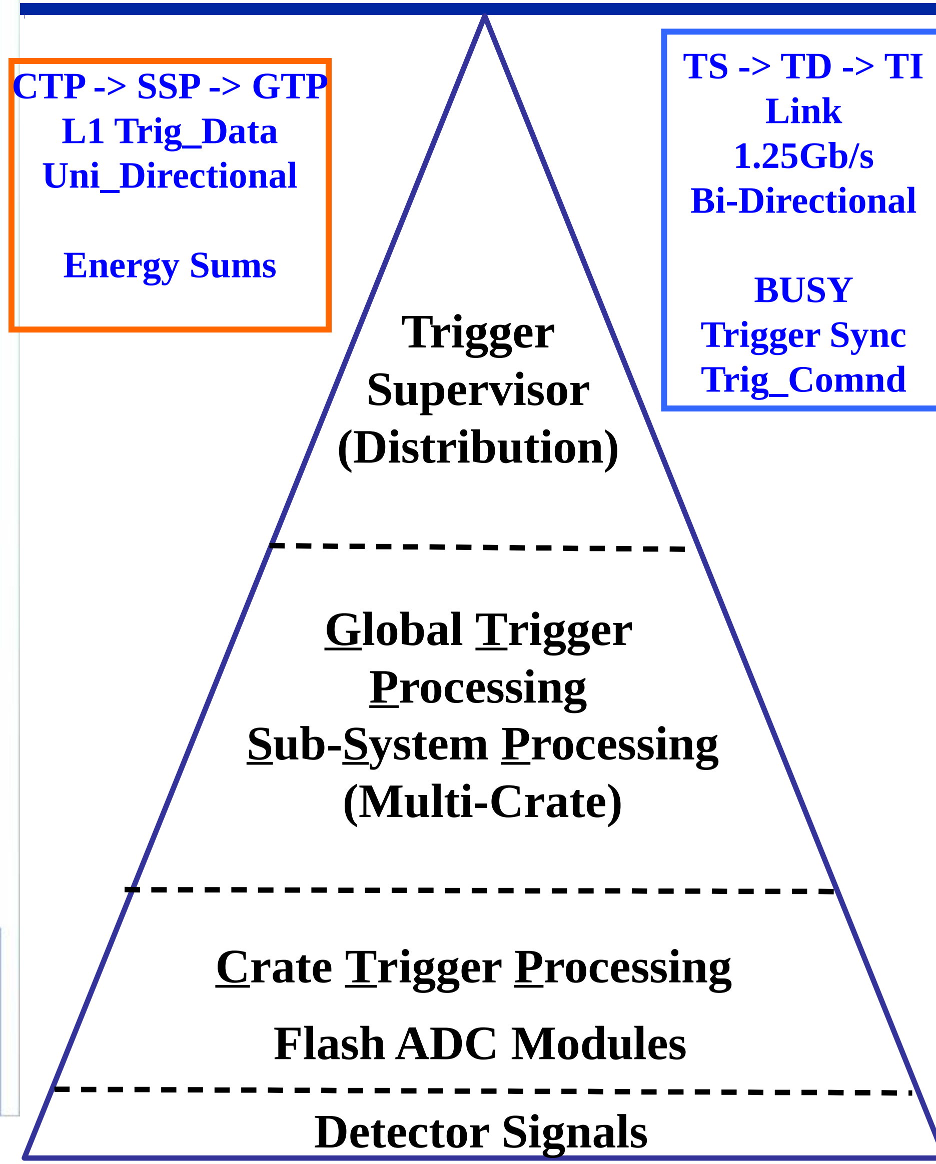


Trigger System Diagram



CTP -> SSP -> GTP
L1 Trig_Data
Uni_Directional

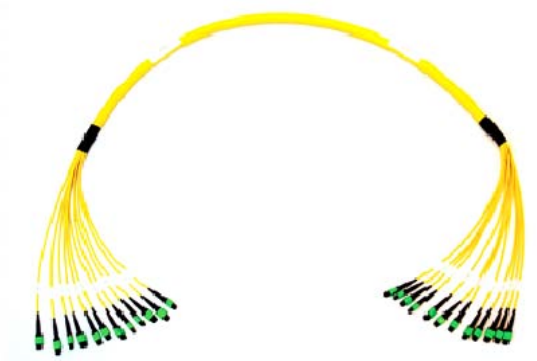
Energy Sums



TS -> TD -> TI
Link
1.25Gb/s
Bi-Directional

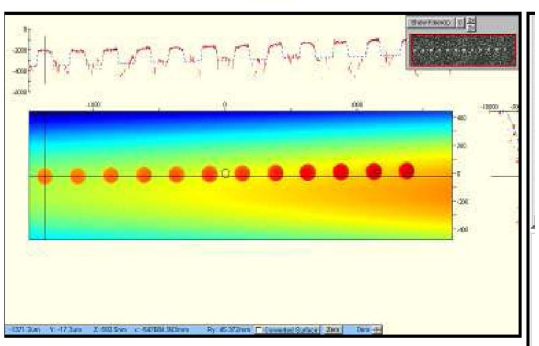
BUSY
Trigger Sync
Trig_Comnd

POP4 Avago Transceivers and MTP parallel fiber cable



- Fiber optic cable has been tested at 150m length
  - Longest optic link is from Hall D to Hall D Tagger
    Is ~100m

- Trunk lines will have 12 parallel ribbon fibers
  - 144 total fibers
  - Multi-mode 50/125um
  - MTP connectors to transceivers and patch panels

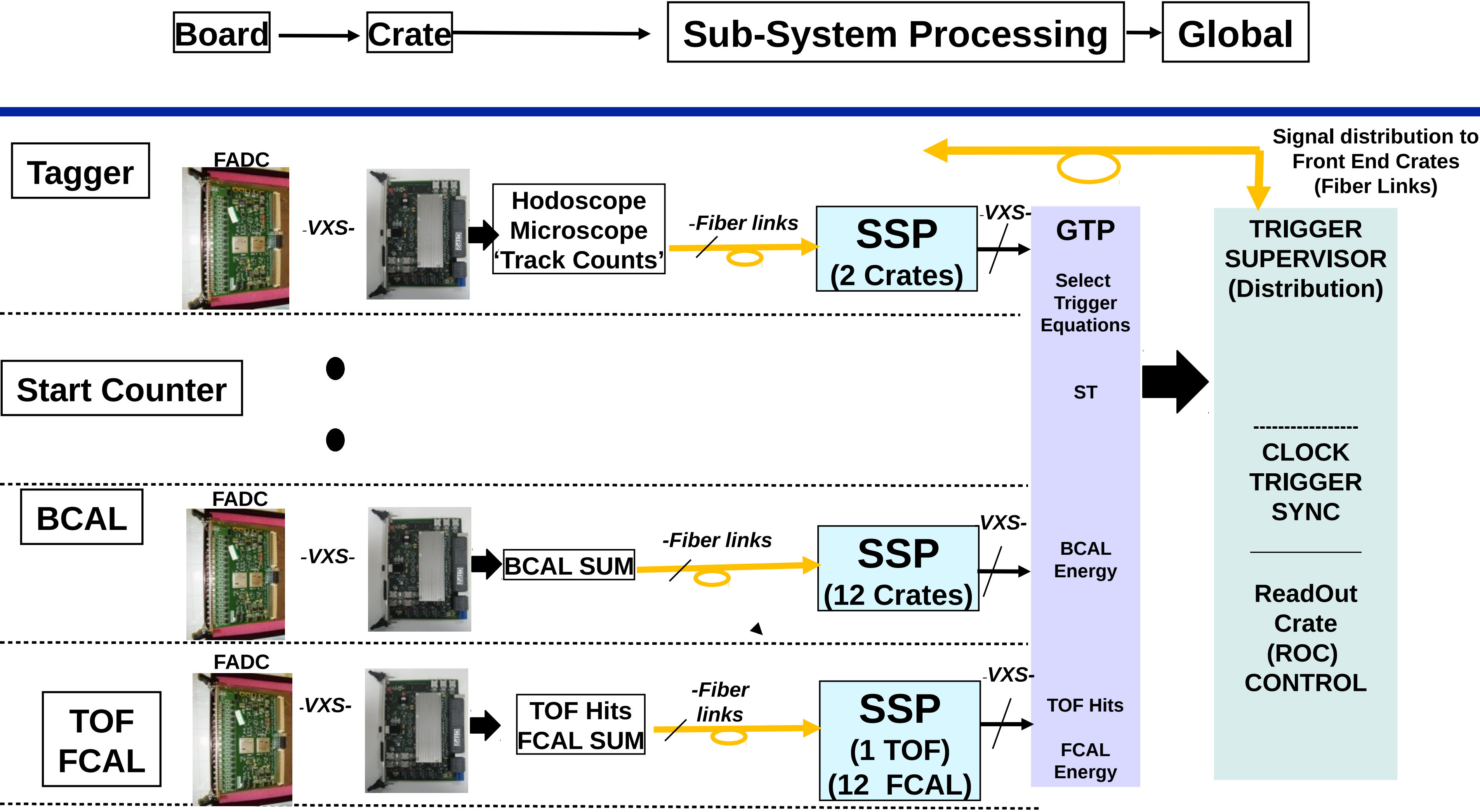


Specifications:

Min insertion loss <0.60db
Wavelength 850nm (Avago POP4 Transceiver 3.125Gb/s)
Attenuation (db/km) - 3.5/1.5
Temperature range: -40C- 80C
Low Smoke Zero Halogen jacket – Non-Plenum tray approved

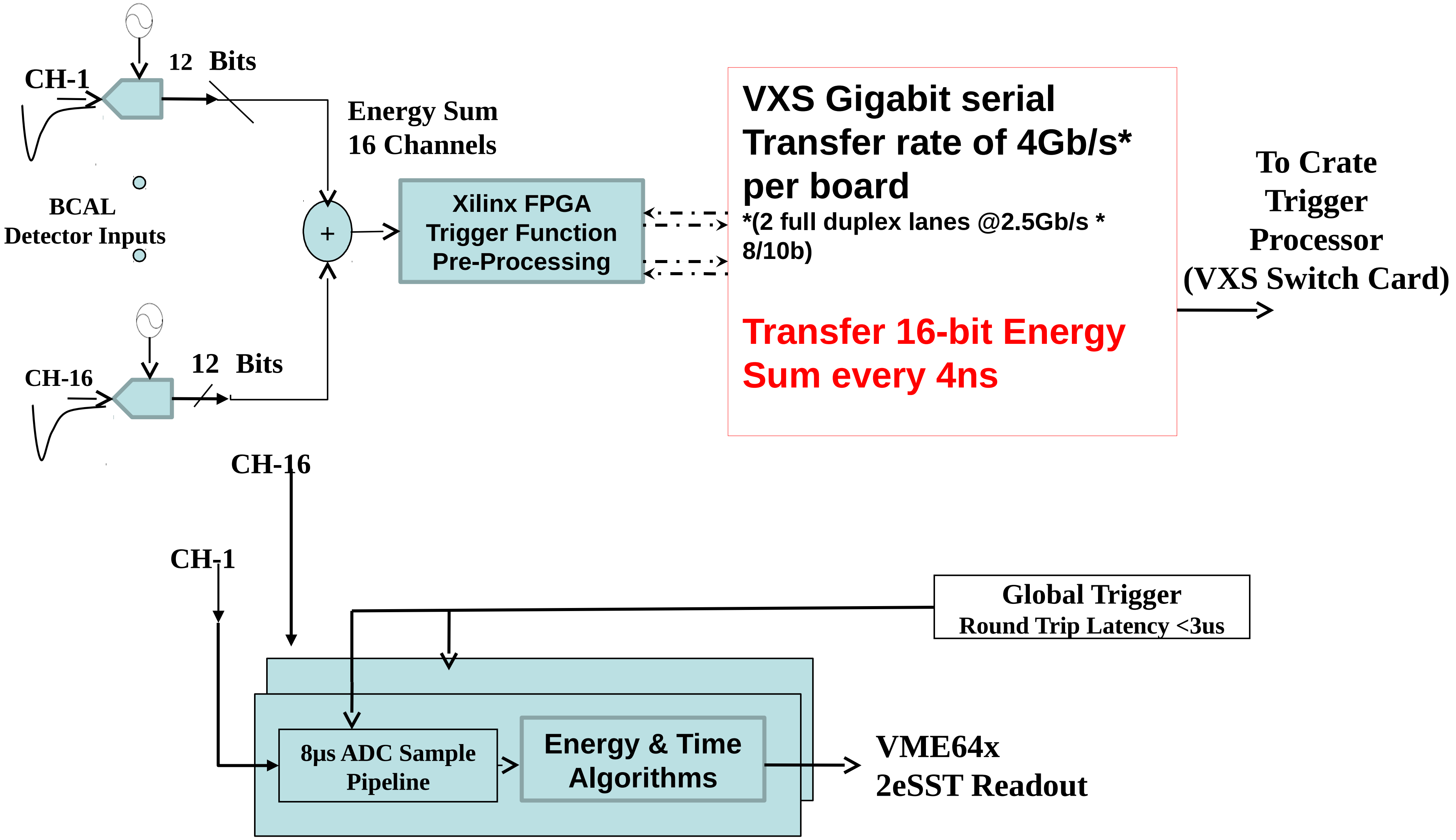
Specifications include installation and testing requirements
Each Hall will require different quantities and specific lengths
Patch panel hardware has been specified and tested

Triggers Arrive Simultaneously on Different Crates with Different Length Fiber Cable



Block Diagram Example:
Hall D Level 1 Trigger

Present Flash ADC Implementation
Energy Sum Trigger



GlueX Example L1 Trigger

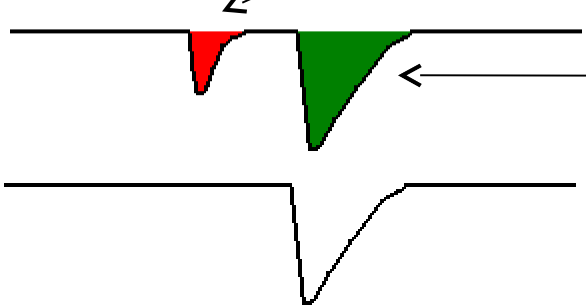
BCAL & FCAL <30MeV Channel Suppression (done at FADC250):

<30MeV – Rejected by FADC250

FADC Channel Input:

>30MeV – Accepted by FADC250

FADC L1 Sum Output:

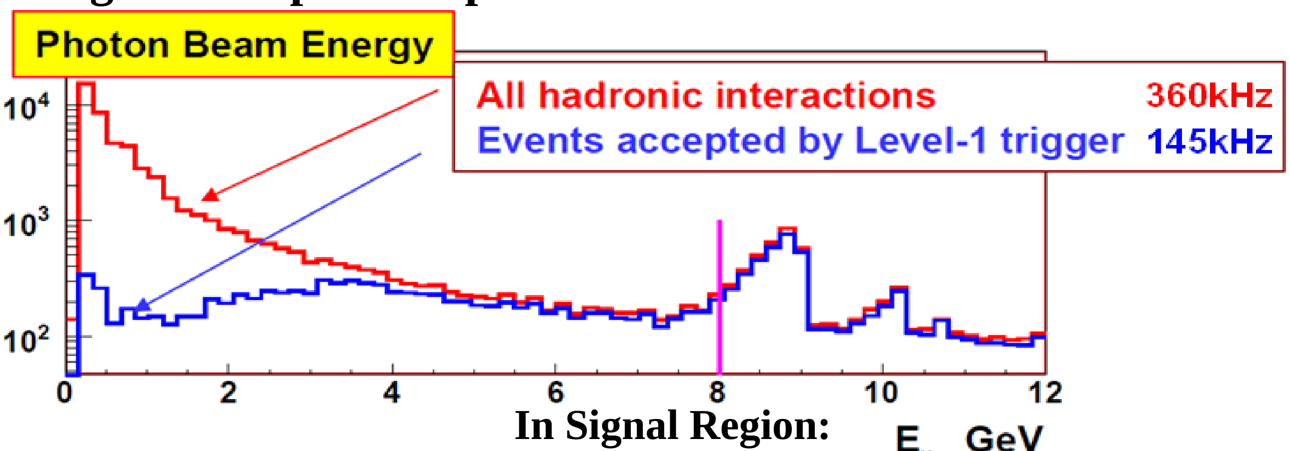


GTP Trigger Equation:

At Luminosity of $10^8\gamma/s$ use the following Trigger equation

$$\sum_{t}^{t+100ns} ST_{hits} > 0 \ \ \&\& \ \ \sum_{t}^{t+100ns} BCAL_{energy} + 4 * FCAL_{energy} > 2GeV$$

Resulting L1 Acceptance Spectrum:

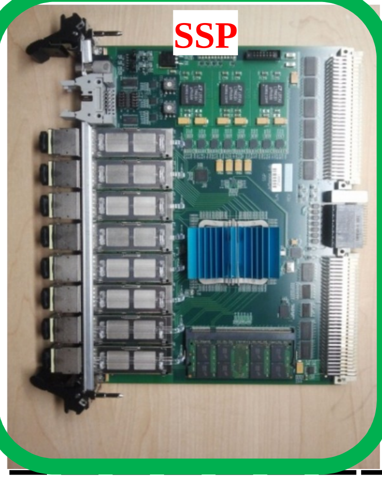


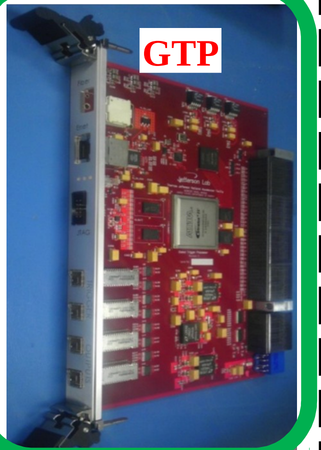
In Signal Region:
L1 Trigger Efficiency > 92%

At Luminosity of $10^7\gamma/s$ Tagger hit counts & Start Counter will be used: L1 Rate ~10KHz

All Trigger Modules Delivered!

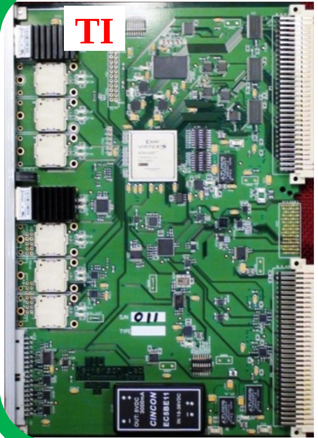
L1 Trigger ‘Data’
MTP Ribbon Fibe



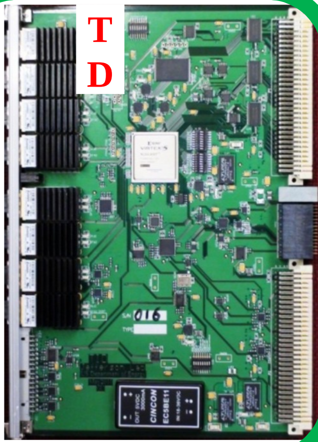


__Global Trigger Crate__

- Sub-System Processor
- Global Trigger Processor



Trigger ‘Link” Control
Clock, Sync
MTP Ribbon Fiber



__Front End Crate__

- FADC250, (FADC125), (F1TDC)
- Crate Trigger Processor
- Signal Distribution
- Trigger Interface

__Trigger Control/Synchronization__

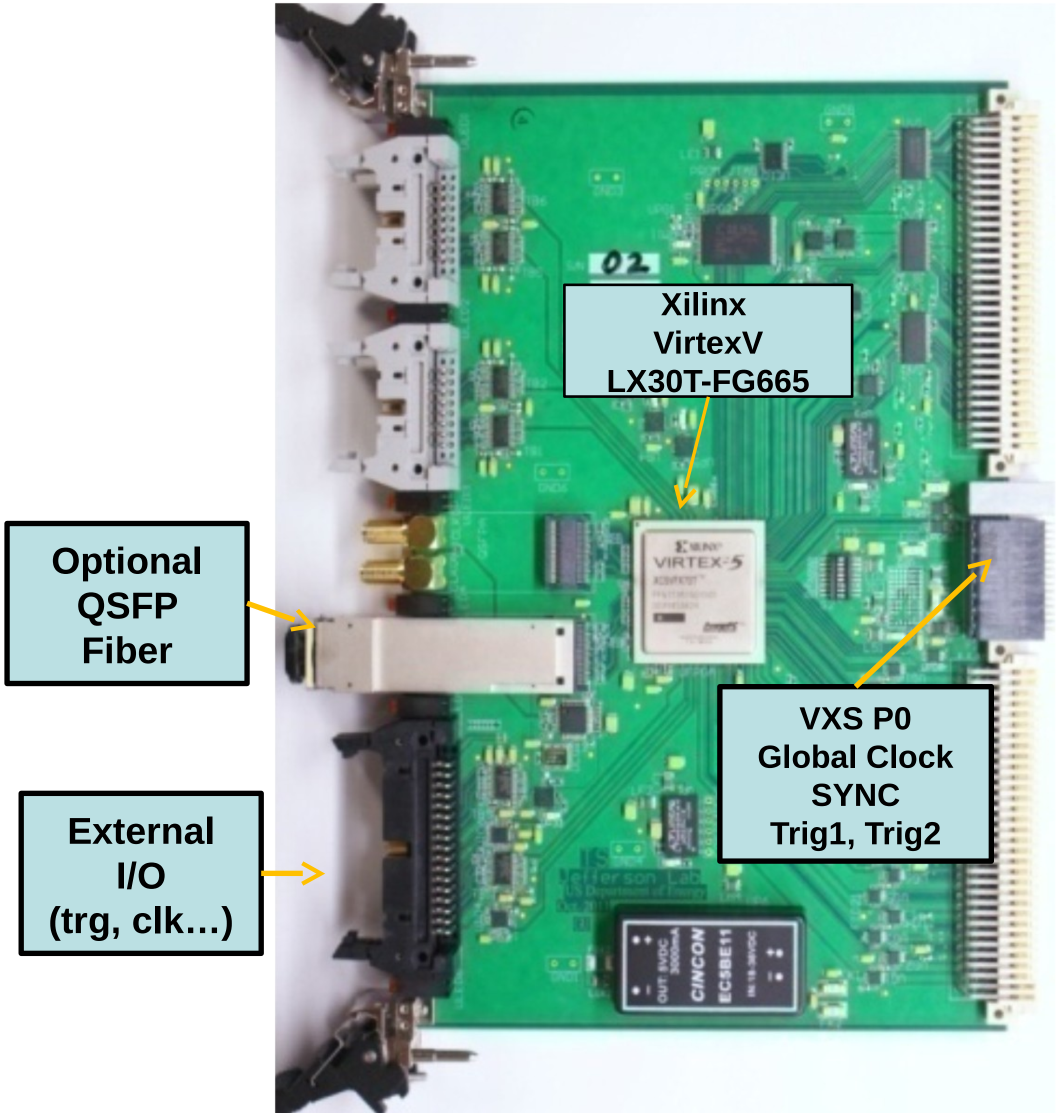
- Trigger Supervisor
- Trigger Distribution

Production Board Quantities

Board ID	Hall D	Hall B	Halls A & C
FADC250	350	310	66
Trigger **I**nterface	64	82	12
Signal **D**istribution	60	53	2
Crate **T**rigger **P**rocessor	30	21	2
Sub-**S**ystem **P**rocessor	10	15	2
Global **T**rigger **P**rocessor	2	2	2
Trigger **D**istribution	8	8	2
Trigger **S**upervisor	2	2	2

Trigger Hardware Status - TS

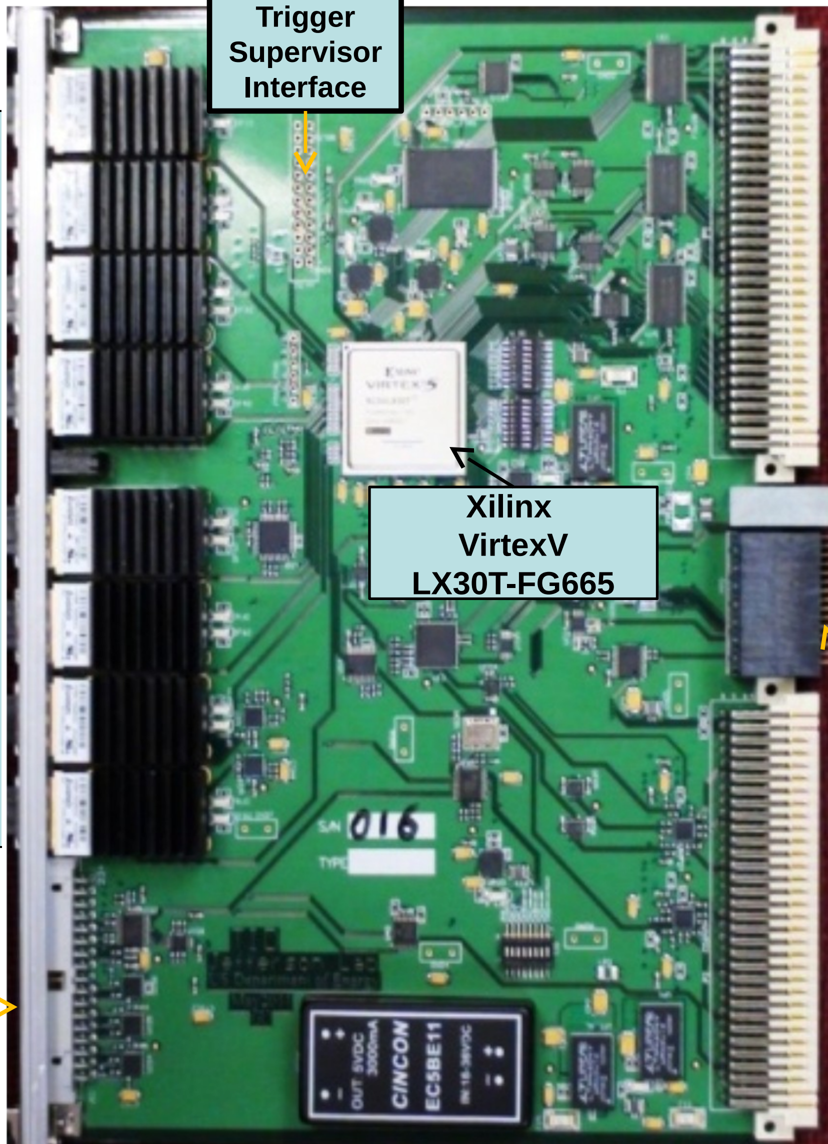
W. Gu
DAQ Group



- **Receives 32 trigger 'Bits' from GTP on P2 via RTM**
- **Global precision clock source connected to SD on VXS backplane**
- **Synchronization and Trigger Word distributed to crate Trigger Interface boards via parallel fiber.**
- **Manages global crate triggers and ReadOut Controller events**
- **VXS "Payload' module**

Trigger Hardware Status - TD

W. Gu
DAQ Group
23-Sept-2011

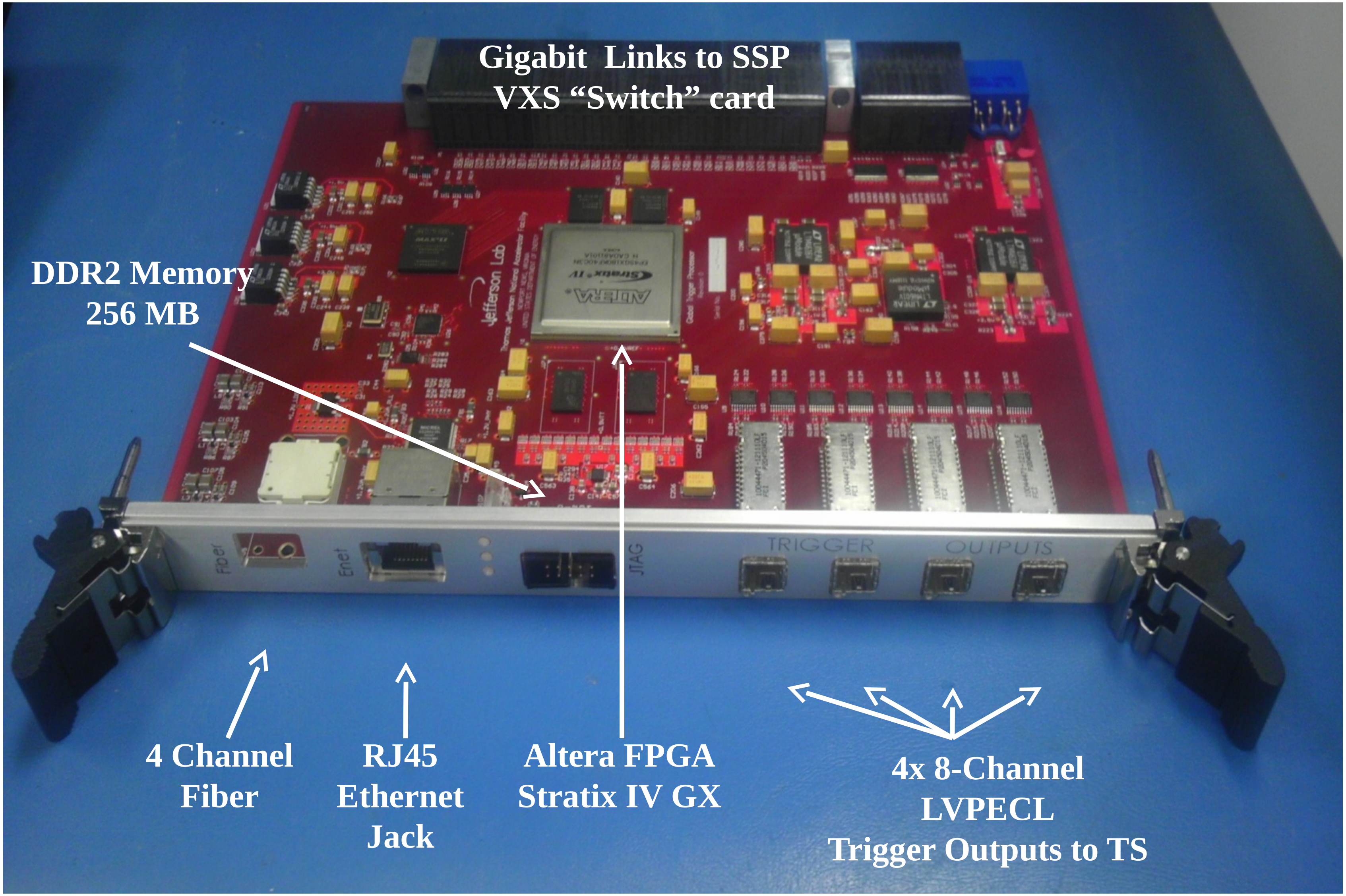


- Distributes from Trigger Supervisor crate to front end crates (TI)
- Distributes precision clock, triggers, and sync to crate TI modules
- Board design supports both TI and TD functions, plus can supervise up to eight front end crates.
- Manages crate triggers and ReadOut Controller events

Trigger Interface "Payload Port 18"

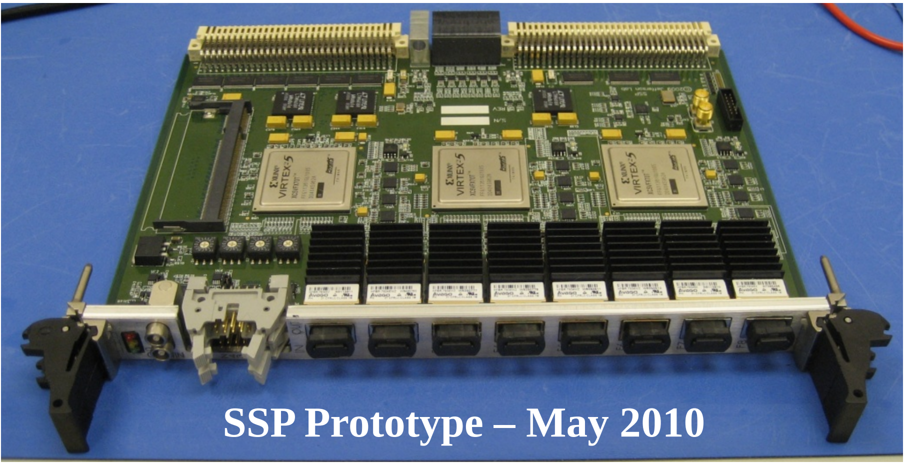
GLOBAL TRIGGER PROCESSOR
1st Article Board

S. Kaneta
2011



Sub-System Processor Status

Ben Raydo



SSP Prototype – May 2010

Production Status:

1) Schematics & BOM complete

 Single FPGA Virtex 5 TX150T

→ New Fiber Transceivers

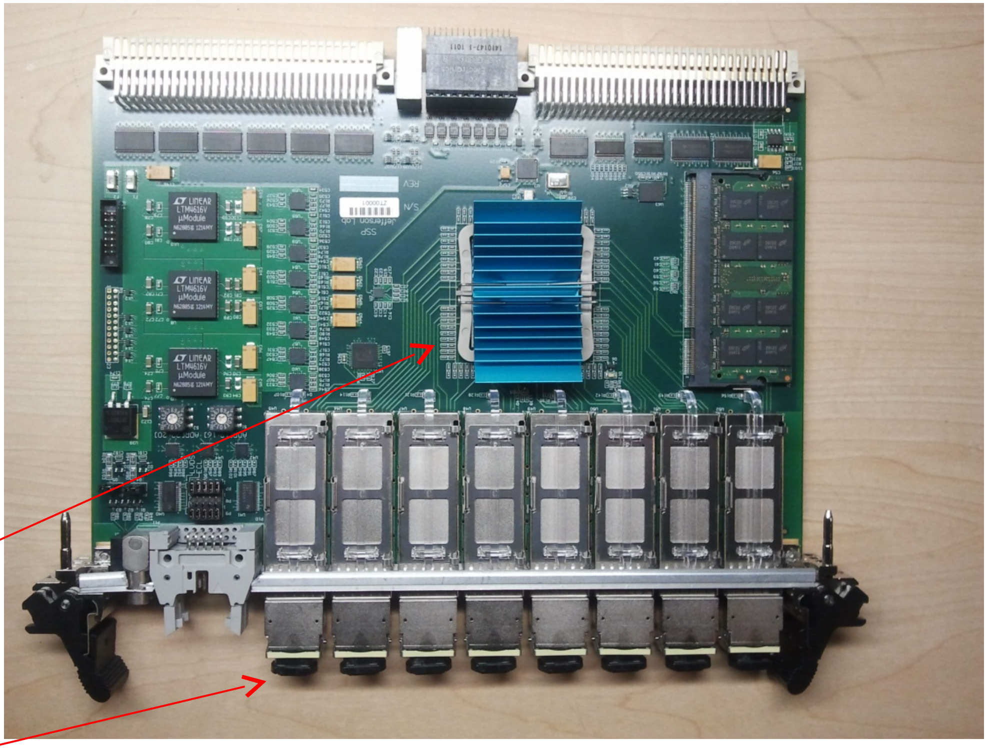
-- Support 10Gb/s (4 ‘Lanes’)

-- Significant cost savings ($40K)

A. Assembly contract awarded

B. Gerbers are ~100% complete, expecting delivery to vendor by Nov 1st.

C. Parts for 1st article arrive Oct 17, 2012… 1st article shipment in December



ALL Production SSP
Delivered and tested

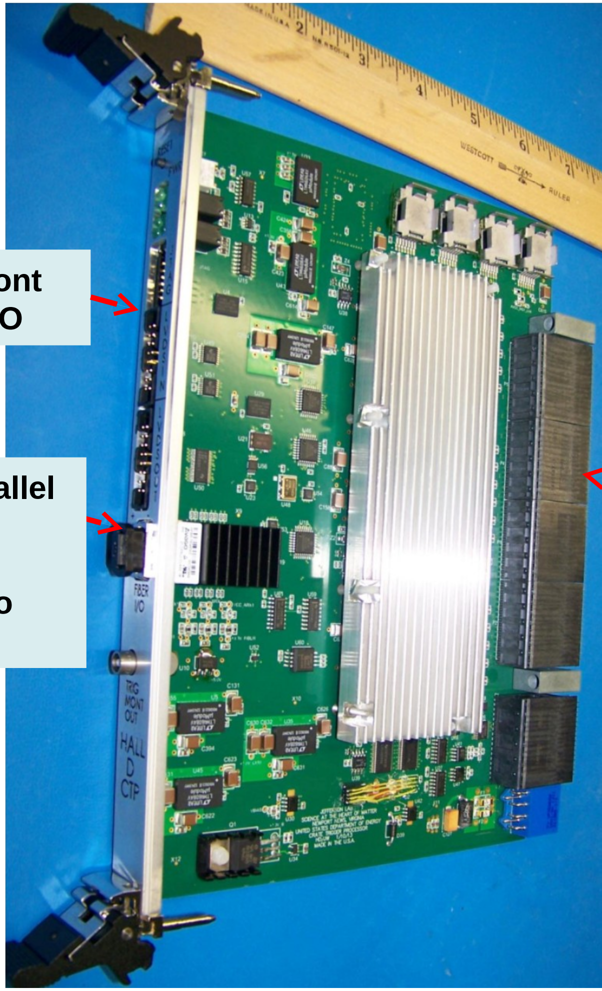
Crate Trigger Processor

Hai Dong
Jeff Wilson

New Front Panel I/O

MTP Parallel Optics

8 Gbps to SSP



VXS Connectors Collect serial data from 16 FADC-250 ***(64Gbps***)

2013 Production CTP

- Crate Trigger Processor (CTP)
  - ✓ Hall D production quantities (32) awarded to MTEQ in Virginia!
  - ✓ 1st Article board passes acceptance testing!
    - Production boards expected delivery 22July2013
      - Latest Virtex V FPGA parts will support 5 Gbps transfer speed with FADC250 and provide additional FPGA resources for future L1 algorithms
  - ✓ Successful operation with HPS calorimeter beam test with latest cluster finding algorithm!!
  - ✓ Sixteen FADC250 boards successfully tested in full crate with FCAT application

N. Nganga

Crate Level – Signal Distribution (SD)

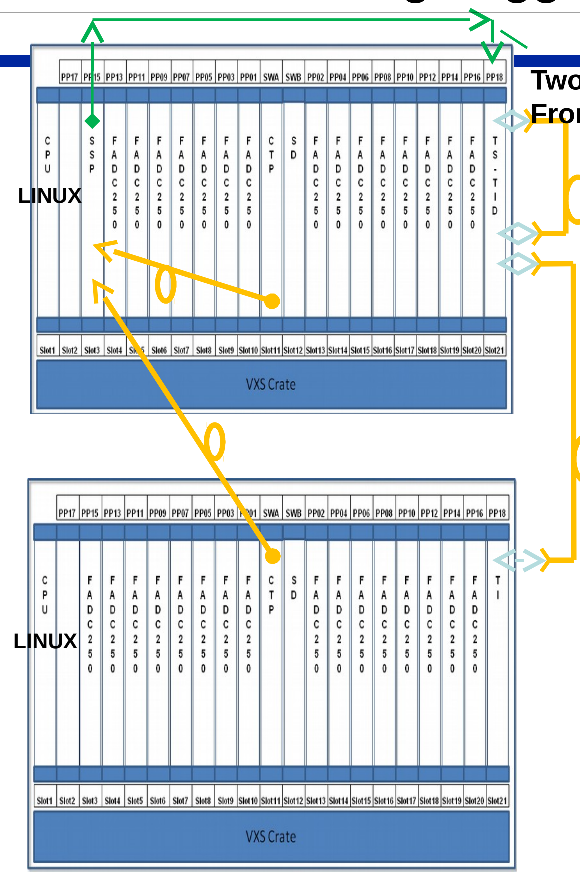
- Clock Jitter attenuation has been tested and distribution to front end payload slots results in ~1.5ps rms Jitter on 250MHz system clock
- SD boards have been used in the two-crate tests since the beginning of Summer 2011 without issues
- Production yield is excellent and only 2 boards (of 115) needed minor assembly rework

Flash ADC 250MHz

- 16 Channel, 12-bit
  - 4ns continuous sampling
  - Input Ranges: 0.5V, 1.0V, 2.0V (user selectable via jumpers)
  - Bipolar input, Full Offset Adj.
  - Intrinsic resolution – σ = 1.15 LSB.
  - 2eSST VME64x readout
  - Several modes for readout data format
    - Raw data
    - Pulse sum mode (Charge)
    - TDC algorithm for timing on LE
  - Multi-Gigabit serial data transport of trigger information through VXS fabric
  - On board trigger features
    - Channel summing
    - Channel coincidence
    - Hit counters
  - Automatic Test Station is complete
  - Production Boards
    - Deliveries on schedule

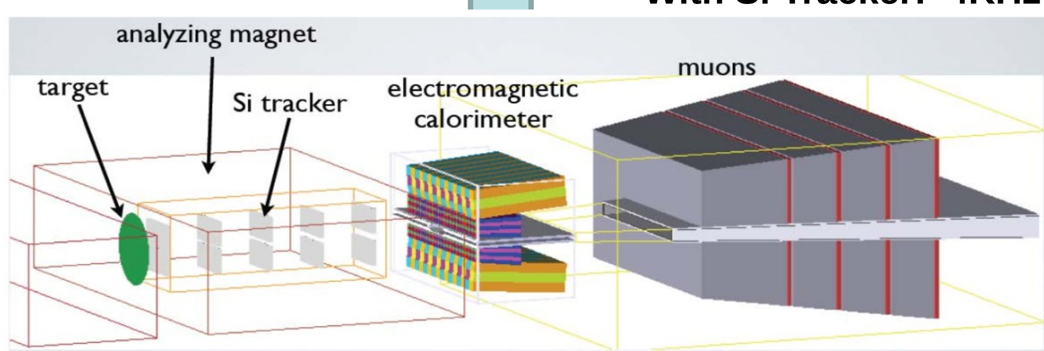
Successful HPS Beam Test with New 12GeV Cluster Finding Trigger App

- **HPS Test Run in Hall B used two full VXS crates**
- **416 APD channels 26 FADC250**
- **Cluster finding algorithm in <u>C</u>rate <u>T</u>rigger <u>P</u>rocessor -- Pushing the resource limit!**
- **New firmware to encode individual channel sums**
- **CTP firmware will report cluster centroid to SSP**
- **SSP will create trigger from CTP output**
- **Exploits the use of the 4Gb/s VXS bandwidth from each FADC250 module**
- **Experiment shows that Hall D L1 Energy Sum algorithm for Calorimetry will clearly 'fit' into CTP**
- **Ebeam 5.55 GeV**
  Radiator 10^-4 r.l. Au
  Collimator 6.4 mm
  Pair spectrometer convertor 1.8x10^-3, 4.5x10^-3 and 1.6x10^-2
  Pair spectrometer field - -760A and +760



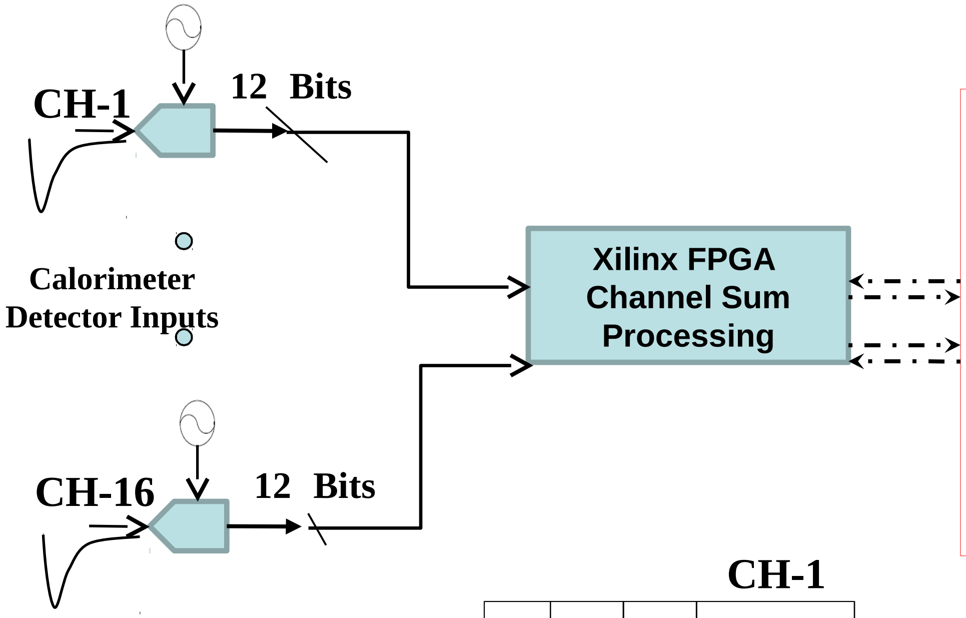
CODA

HPS DAq rates:
Ecal +20KHz
With Si Tracker: 4KHz



Heavy Photon Search Collaboration

Trigger Data Encoding Format
HPS Experiment

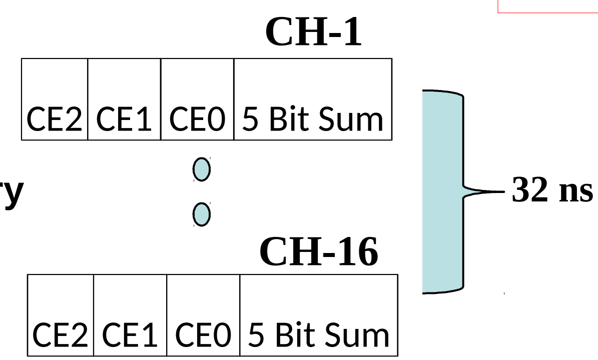


VXS Gigabit serial fabric
Transfer rate of *4Gb/s* per board
(2 full duplex lanes @2.5Gb/s)

Use 32ns ‘frame’ to Transfer 16-bytes
Each channel is 1 byte:
5 bit Sum + 3 bits for timing

To Crate Trigger Processor (VXS Switch Card)

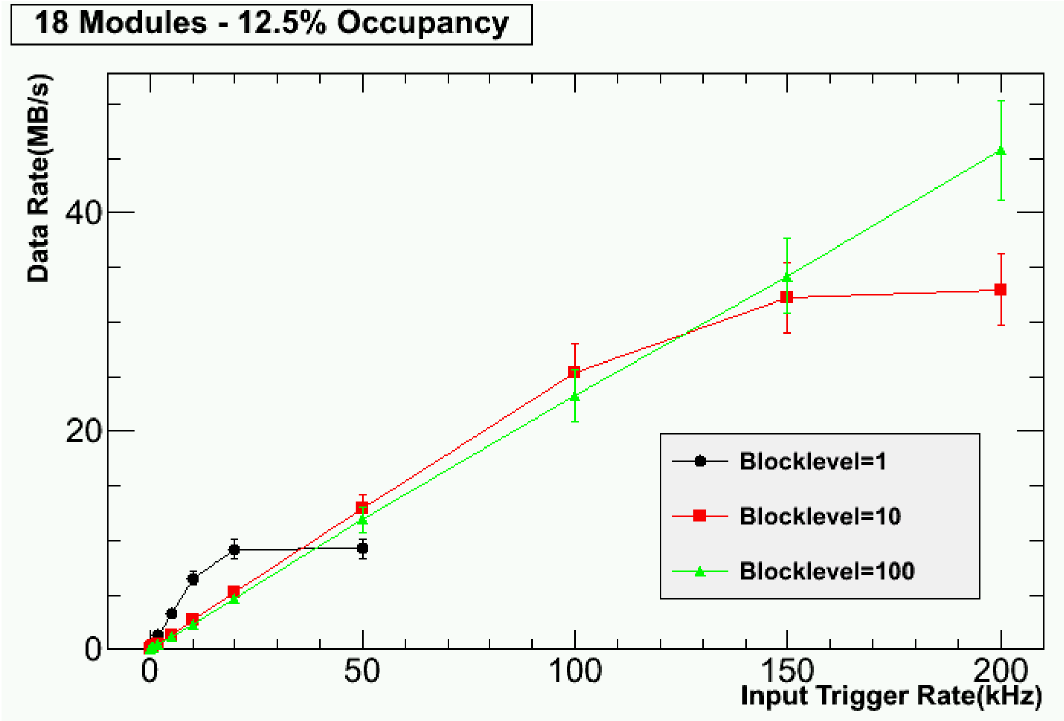
3 bit clock encoding
Allows 4ns clock recovery
in 32ns ‘frame’



16 Bytes in 32ns
Meets the *4Gb/s*
transfer
bandwidth
Per board

DAq Trigger & Readout Performance

- System testing includes:
  - Gigabit serial data alignment
    - ✓ 4Gb/s from each slot
    - ✓ 64Gb/s to switch slot
    - ✓ Crate sum to Global crate @8Gb/s
  - Low jitter clock, synchronization
    - ✓ ~1.5ps clock jitter at crate level
    - ✓ 4ns Synchronization
  - Trigger rate testing
  - Readout Data rate testing
  - Overall Trigger Signal Latency
    - ✓ ~2.3us (Without GTP and TS)



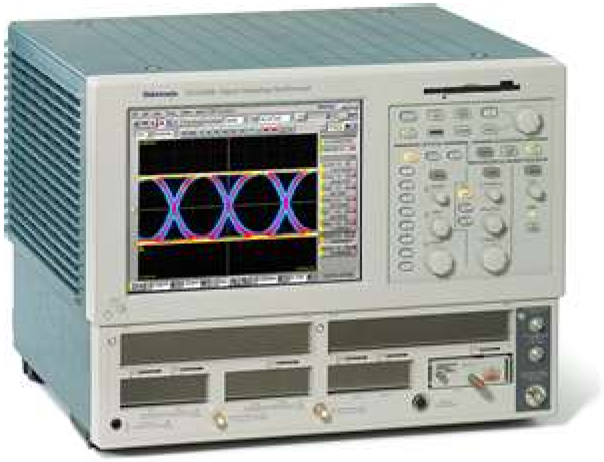
200KHz Trigger Rate!

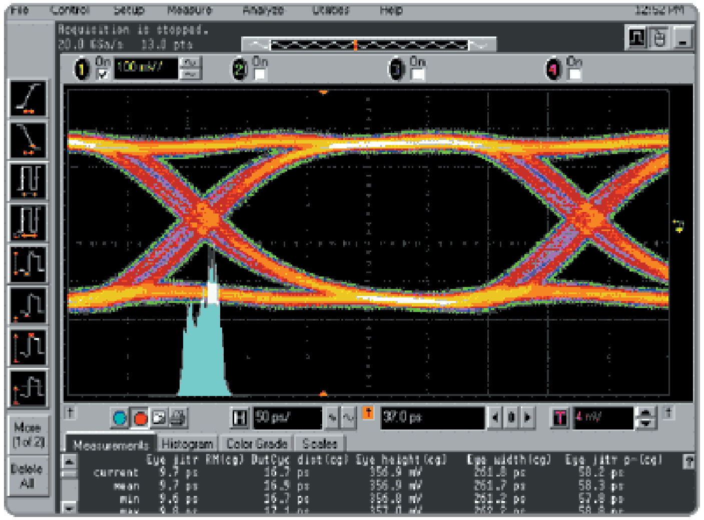
Readout Controller Capable of 110MB/s
- Testing shows we are well within limits

Summary

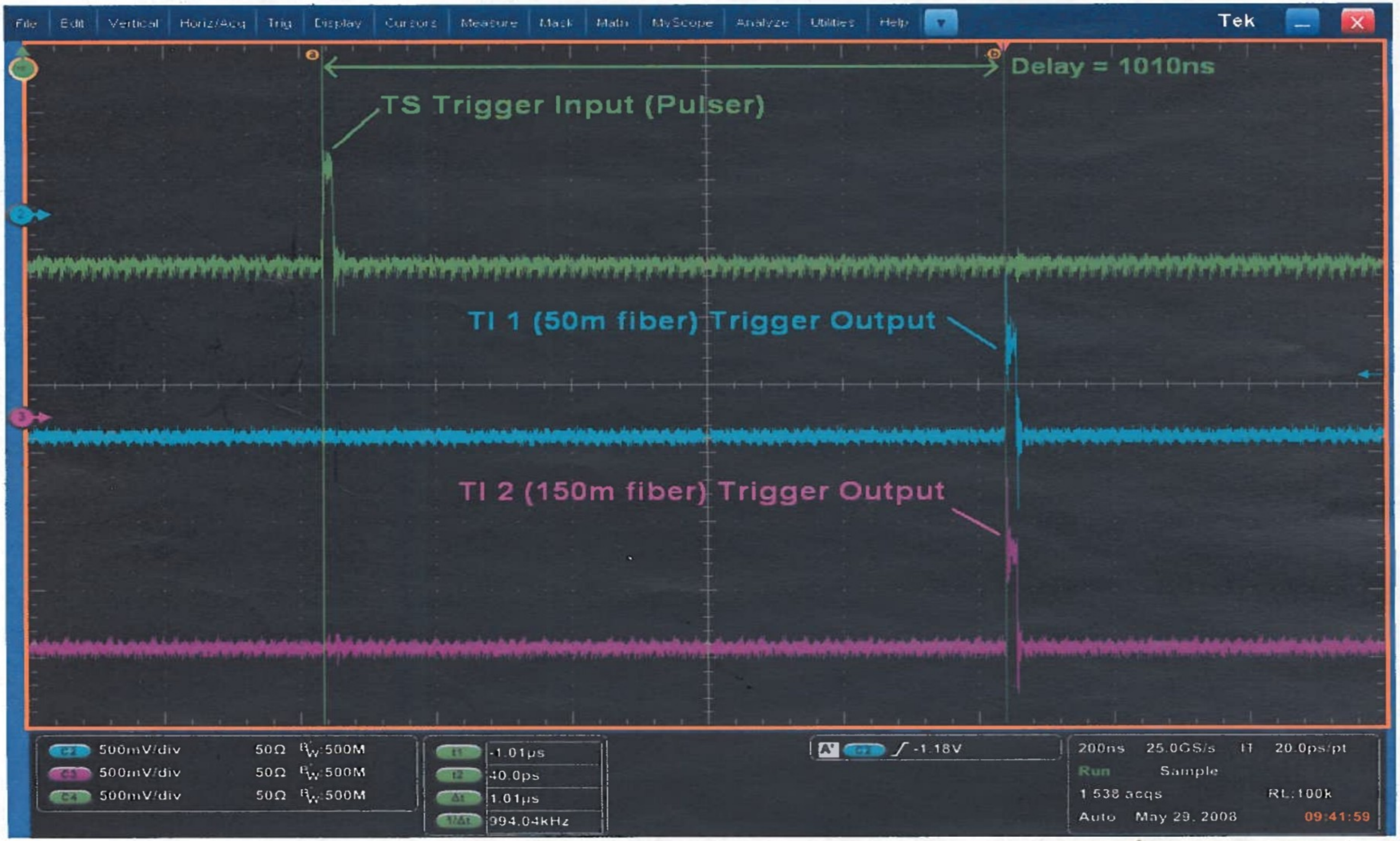
- **FY12 production board schedules on track**
  - **Production order for GTP and TS remain**
  - **GTP and TS pre-production units are fully functional**
    - **Global Crate testing has started**
    - **Parallel fiber optic transceivers/cable type has been tested**
  - **Fiber and patch panels/cable have been ordered and received for Hall C**
- **Two full crate DAq system used successfully for the Heavy Photon Search test in Hall B. (May 2012)**
  - **Excellent test foundation for software drivers, new calorimeter trigger algorithms and detector commissioning tools.**
  - **Cluster finding Trigger application performance exceeds Energy summation function required for other experiments.**
- **Full crate hardware acceptance testing in progress**
  - **Verification of all boards in final crate configuration**
- **<u>Infrastructure and Engineering support/expertise exists for post CD4 Ops</u>**

Backup slides





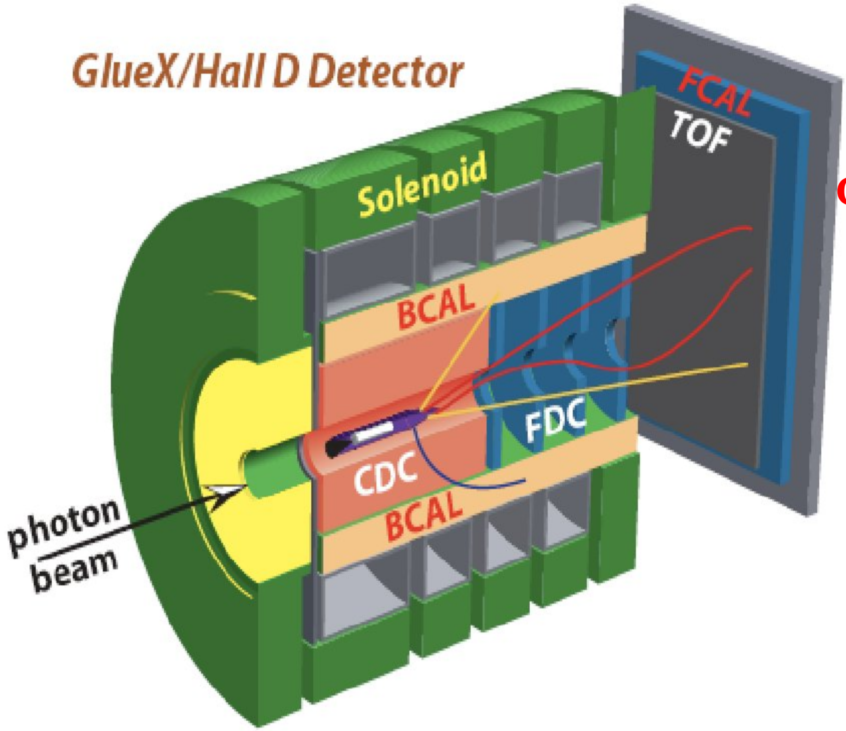
Trigger Distribution Delay

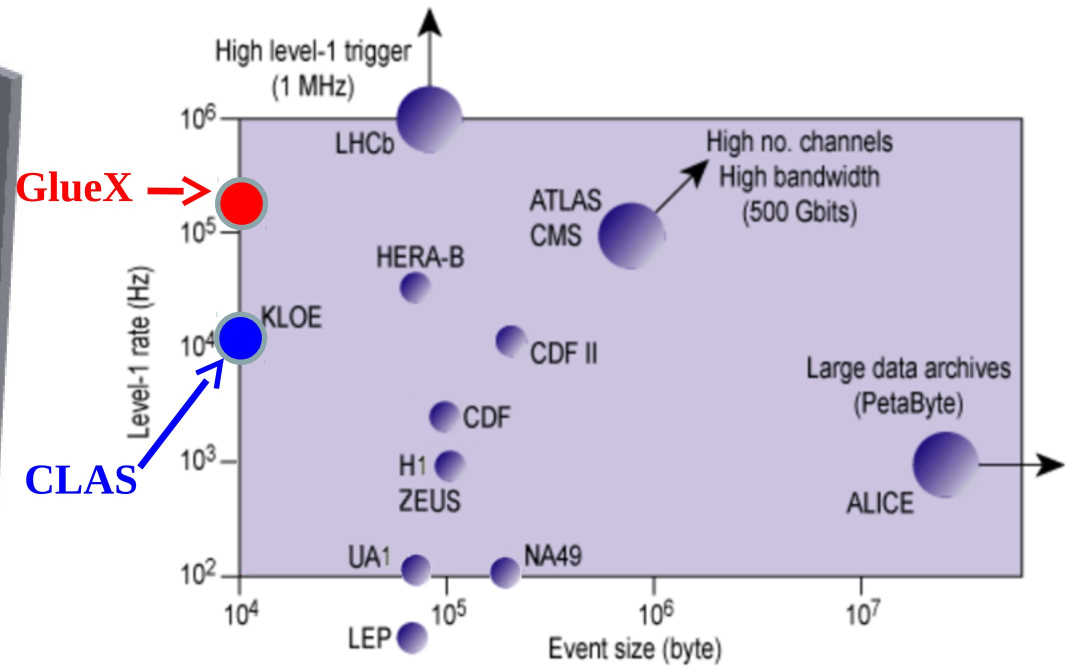


Production Test Plans

Board ID	Status	Acceptance Procedure Complete?
FADC250	Production Board Deliveries on Schedule	Yes
Trigger **I**nterface	Production Board Deliveries on Schedule	Yes
Signal **D**istribution	ALL boards delivered and tested	Yes
Crate **T**rigger **P**rocessor	Production Board awarded Due Feb-2013	Yes
Sub-**S**ystem **P**rocessor	Production Boards awarded Due Jan-2013	Yes
Global **T**rigger **P**rocessor	2 Pre-Production units fully functional	In Development
Trigger **D**istribution	Production Board Deliveries on Schedule	Yes
Trigger **S**upervisor	2 Pre-Production units fully functional	In Development

GlueX comparison to CLAS in Hall B

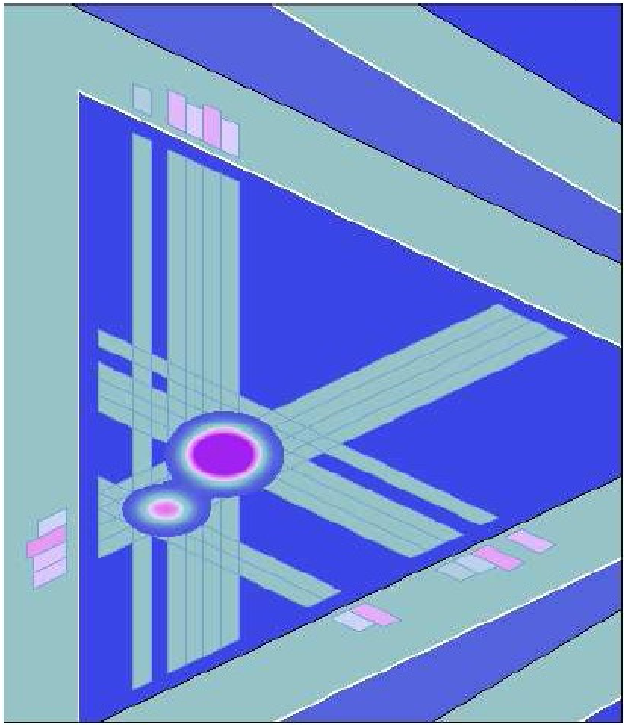




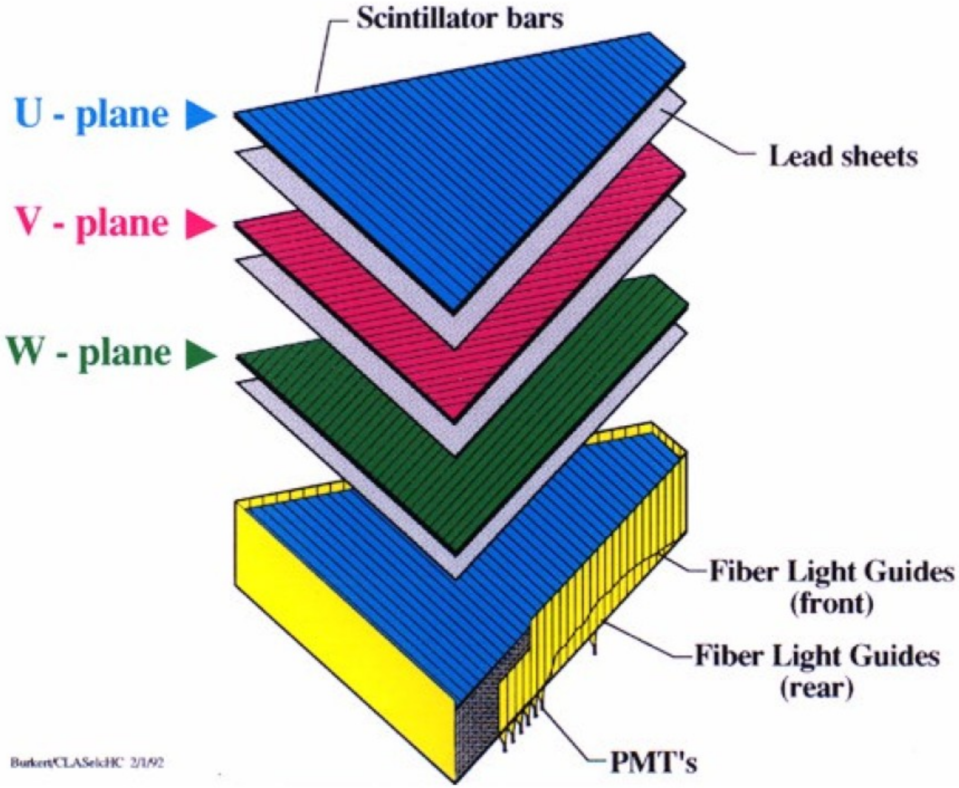
	Hall D-GlueX	Hall B-CLAS
Channel Count:	~20k	~40k
Event Size:	~15kB	~6kB
L1 Rate:	200kHz	10kHz
L1 Data:	3GB/s	60MB/s
To Disk:	L3, 20kHz, 300MB/s	L2, 10kHz, 60MB/s

5.7 Ex: Forward Calorimeter Cluster Finding

Calorimeter cluster reconstruction (1 sector shown):



Calorimeter construction:



- Cluster reconstruction will be formed in L1 trigger level and matched with drift chamber tracks for each sector.

More 12GeV Electronics support activities

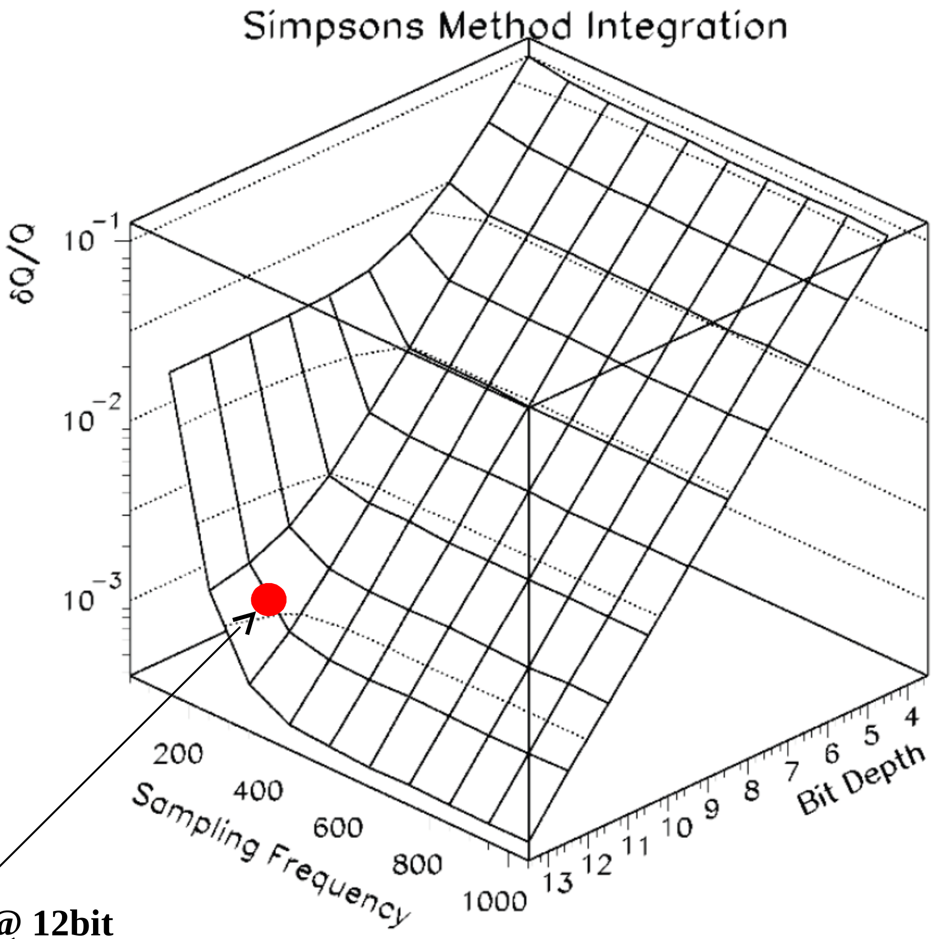
Specific to Hall D: (F. Barbosa, C. Stanislav, N. Sandoval, C. Dickover, A. Stepanyan, J. Wilson, E. Jastrzembski(DAQ))

- **F1TDC – Two versions: 32 channel high resolution; 48 channel normal resolution**
  - **Production versions have been ordered and will be tested at UMass**
- **FADC125 – Production boards awarded and deliveries have started**
- **Significant production/assembly work at JLAB on the SiPM circuits for BCAL, Start Counter and Pair Spectrometer detectors**
- **FDC, CDC, circuit board design, inspection, testing, analysis, and installation**
- **Installation, schedules, coordination with collaborating institutions**
  - ➢ **Preparations for full crate DAq testing with production boards (F112)**
  - ➢ **12 full crates installed in the Hall D counting house for CODA/DAq/Trigger testing.**
- **Electrical safety guidance and review**

3.4 FADC Sampling – Charge Accuracy

Hall D FCAL PMT: FEU 84-3

- **10,000 Random height pulses 10-90% full scale of ADC range simulated**
- **Sampling frequency makes little difference beyond 250MHz at 12bit, providing ~0.1% charge resolution**
- **PMT pulse shape dominates sample frequency and bit depth of ADC**



250MHz @ 12bit

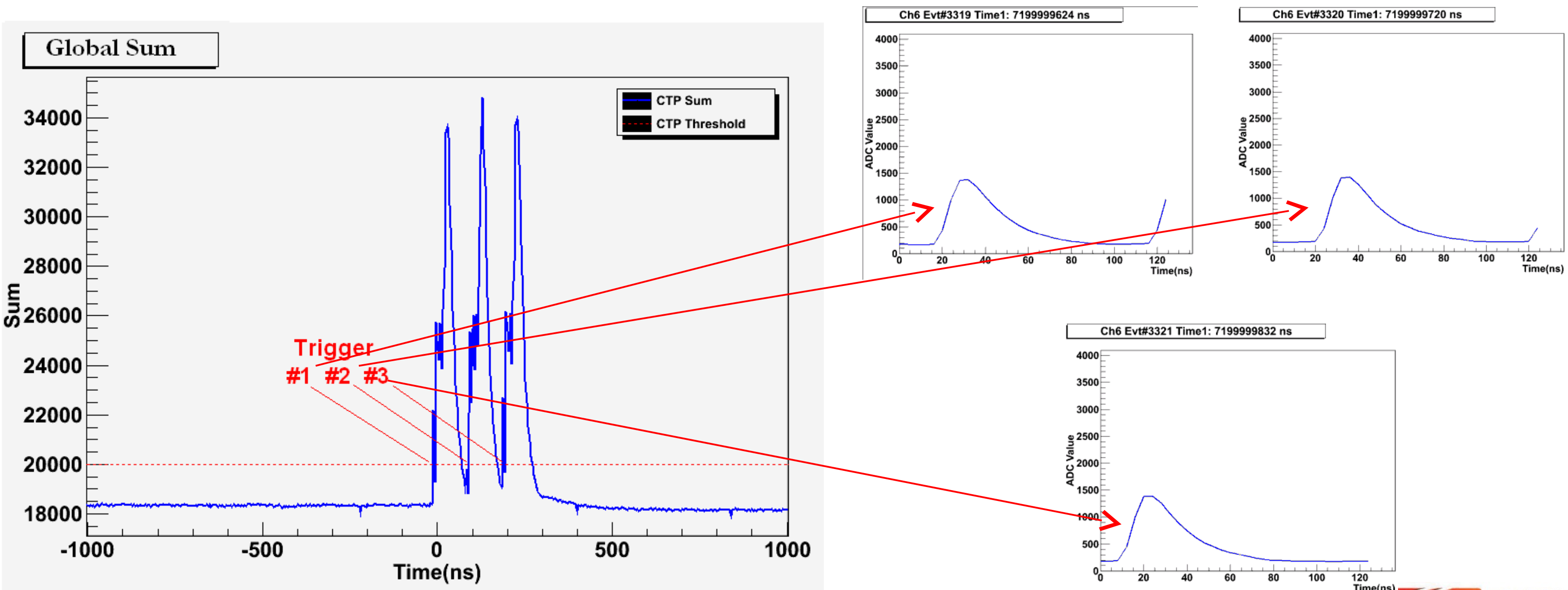
From: 33 Doc# 425-v1

Synchronized Multi-Crate Readout

- CTP #2 is also acting as an SSP (by summing the local crate + CTP#1 sum over fiber
- A programmable threshold is set in CTP, which creates a trigger when the global sum (6 FADC boards => 96 channels) is over threshold.
- Example test with a burst of 3 pulses into 16 channels across 2 crates/6 FADC modules

A 2µs global sum window is recorded around the trigger to see how the trigger was formed:

Example Raw Event Data for 1 FADC Channel:

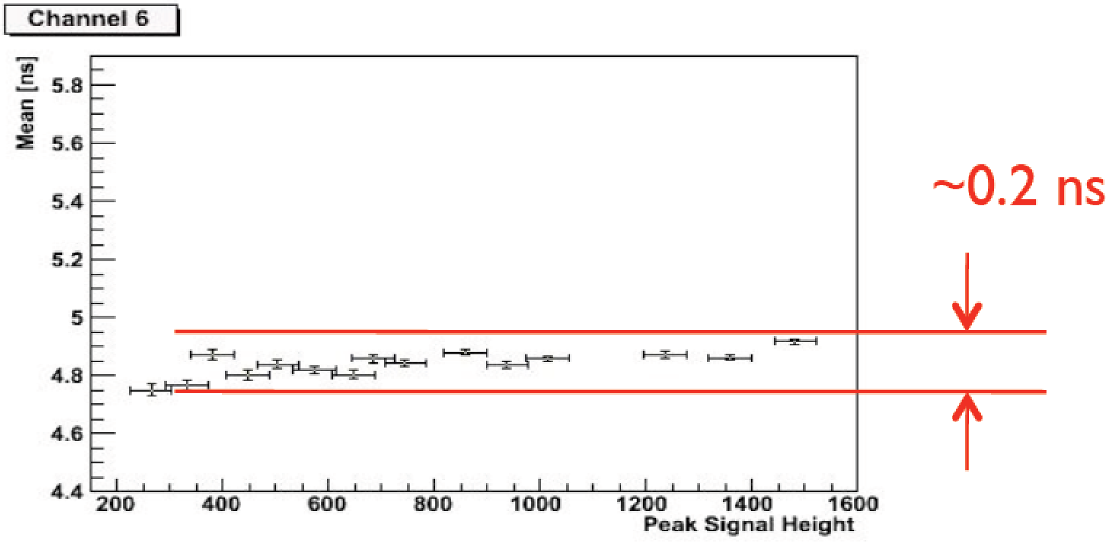


FADC Sampling – Timing Accuracy

Hall D FCAL PMT: FEU 84-3

- **Timing algorithm developed & tested by Indiana University for the Hall D forward calorimeter.**
- **Implemented on the JLab FADC250 hardware achieving <300ps timing resolution on 50% pulse crossing time with varied signal heights.**

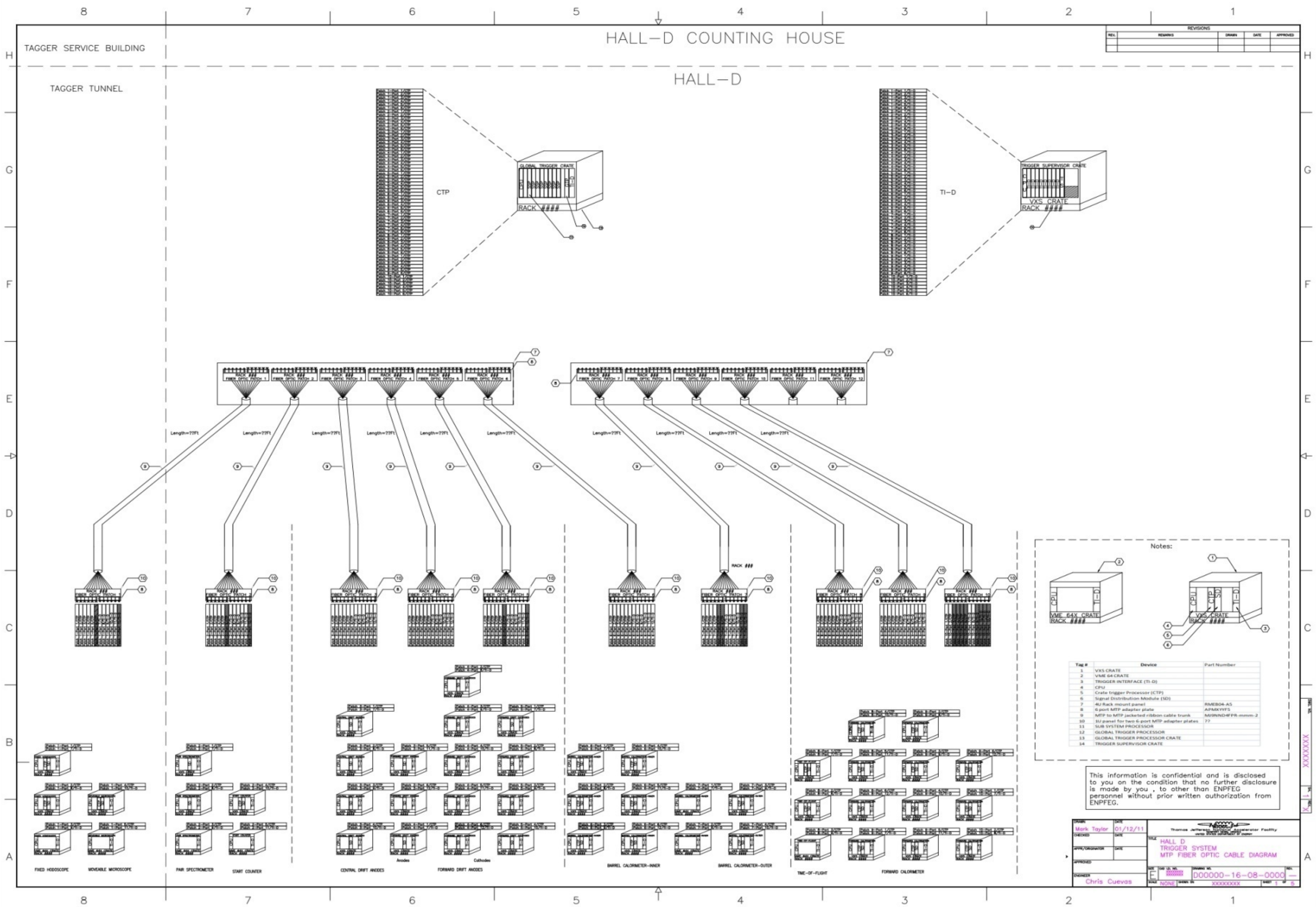
- Resolution allow reliable information to link calorimeter with tagged electron bunch.



Typical timing resolution achieved ~1/10 the sample rate. The PMT shape will drive the ADC sample rate & depth requirements.

From: GlueX Doc# 1258-v1

Trigger System – Fiber Optic Diagram



CLAS12 Data Acquisition System

- 3724 channels of 12bit 250MHz Flash ADCs
- 3724 channels of 85ps and 35ps resolution pipeline TDCs with discriminators collecting data from:
  - 2 Calorimeters per sector – PCAL, ECAL
  - 2 Cerenkov counters – HTCC, CC/sector
  - Time-of-flight detectors – CTOF, TOF/sector
- All electronics is compatible with pipelined DAQ concept
- 24192 channels from Drift Chambers (TDC w/1ns LSB)
  - Drift Chamber Readout Board with Tracking Trigger Features
- Central tracker readout system
- >50 VME/VME64X/VXS crates equipped with Readout Controllers and Trigger Interface Units
- JLAB Trigger System Modules
  - Benefit from Hall D 200KHz Trigger rate design requirement
- JLAB CODA DAQ software